Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title conforms to the claimed matter.

The new claims obviate the rejections under 35 USC 103. The new claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

New claim 25 defines a first-in first-out memory.

Memory circuitry has word storage slots. Each word storage slot contains a same certain number of bits. The memory circuitry has a read pointer address input and a write pointer address input.

Data read/write circuitry has a parallel port selectively coupled with each word storage slot, a system data path, a control input, and a scan data input/output.

Control circuitry has a read pointer address output connected with the read pointer address input and a write pointer address output connected with the write pointer address input. The control circuitry has a control output connected with the control input of the data read/write circuitry and a scan control output.

Scan storage circuitry is separate from the memory circuitry. The scan storage circuitry has a serial input, a serial output, a scan data output/input connected with the scan data input/output of the data read/write circuitry, and a control input connected with the scan control output.

In contrast, US 6,343,358 to Jagger discloses:

> Apparatus for processing data is provided, said apparatus comprising: a main processor 4; an instruction transfer register ITR for holding a data processing instruction and accessible via a first serial scan chain SC4; a data transfer register DTR for holding a data value and accessible via a second serial scan chain SC5; debug logic 6, 12 for controlling said main processor 4, said instruction transfer register ITR and said data transfer register DTR such that a data processing instruction held within said instruction transfer register ITR is passed a plurality of times to said main processor 4 for execution upon a sequence of data values scanned into or from said data transfer register via said second serial scan chain. In this way operational speed of the debug mode is increased since the data processing instruction only needs to be transferred once. Abstract

The Jagger patent thus discloses an instruction transfer register accessible through a first serial scan chain and a data transfer register accessible through a second serial scan chain. The Jagger patent fails to teach or disclose a scan storage circuit separate from word storage slots in a FIFO memory.

New claim 25 distinguishes over the Jagger patent with the limitations of a first-in first-out memory comprising memory circuitry having word storage slots, each word storage slot containing a same certain number of bits, and having a read pointer address input and a write pointer address input; data read/write circuitry having a parallel port selectively coupled with each word storage slot, a system data path, a control input, and a scan data input/output; control circuitry having a read pointer address output

connected with the read pointer address input and a write pointer address output connected with the write pointer address input, the control circuitry having a control output connected with the control input of the data read/write circuitry, and having a scan control output; and scan storage circuitry separate from the memory circuitry, the scan storage circuitry having a serial input, a serial output, a scan data output/input connected with the scan data input/output of the data read/write circuitry, and a control input connected with the scan control output.

US 6,848,042 to Campbell discloses:

> A method of outputting data from a FIFO incorporated in an integrated circuit generally determines whether input data is valid during a first clock cycle. The method then outputs data from a plurality of output barrel slots during a second clock cycle. Data is then shifted from predetermined upper barrel slots to predetermined output barrel slots during second cycle based upon a barrel count. Finally, data is shifted into the FIFO during said second cycle based upon the barrel count. A new barrel count of valid data in the FIFO can then be determined. Circuitry for implementing the embodiments of the invention is also disclosed. Abstract

The Campbell patent thus discloses a process of outputting and inputting data in a FIFO using barrel counts. The Campbell patent fails to teach or disclose a scan storage circuit separate from word storage slots in a FIFO memory.

New claim 25 distinguishes over the Campbell patent with the limitations of a first-in first-out memory comprising memory circuitry having word storage slots, each word storage slot containing a same certain number of bits, and having a read pointer address input and a write pointer address input; data read/write circuitry having a parallel port selectively coupled with each word storage slot, a system data path, a control input, and

a scan data input/output; control circuitry having a read pointer address output connected with the read pointer address input and a write pointer address output connected with the write pointer address input, the control circuitry having a control output connected with the control input of the data read/write circuitry, and having a scan control output; and scan storage circuitry separate from the memory circuitry, the scan storage circuitry having a serial input, a serial output, a scan data output/input connected with the scan data input/output of the data read/write circuitry, and a control input connected with the scan control output.

US 5,995,988 to Freidin discloses:

> An apparatus for loading configuration information into a programmable integrated circuit (e.g., an FPGA) configurable to perform parallel loading or bit serial loading within the same architecture. The configuration information is presented to the FPGA in data frames of N serial bits each. Each data frame is divided into discrete serial portions having Y bits each (e.g., a data frame comprises N/Y portions). In parallel mode, the portions are loaded into a segmented configuration register, one portion per programming cycle, such that Y bits are loaded into the segmented configuration register in parallel. On each programming clock cycle during parallel loading, all the bits of a data frame portion are simultaneously loaded into the segments of the configuration register (at the first bit position for each segment) such that each segment receives one bit per programming cycle. The bits of the configuration register are then shifted down by one and the cycle repeats for the next data frame portion. Under this mechanism, Y bits are loaded in parallel into the configuration register for increased transfer rate. The architecture of the novel configuration register is such that it is configurable in a serial mode to receive a single serial bit stream of the N bit data frame for downward compatibility. Abstract

The Freidin patent thus discloses configuring a FPGA. The Freidin patent fails to teach or disclose a scan storage circuit separate from word storage slots in a FIFO memory.

New claim 25 distinguishes over the Freidin patent with the limitations of a first-in first-out memory comprising memory circuitry having word storage slots, each word storage slot containing a same certain number of bits, and having a read pointer address input and a write pointer address input; data read/write circuitry having a parallel port selectively coupled with each word storage slot, a system data path, a control input, and a scan data input/output; control circuitry having a read pointer address output connected with the read pointer address input and a write pointer address output connected with the write pointer address input, the control circuitry having a control output connected with the control input of the data read/write circuitry, and having a scan control output; and scan storage circuitry separate from the memory circuitry, the scan storage circuitry having a serial input, a serial output, a scan data output/input connected with the scan data input/output of the data read/write circuitry, and a control input connected with the scan control output.

Claim 25 stands allowable.

Claim 29 defines a process of scan testing a first-in first-out memory having word storage slots.

The process sets a read pointer and a write pointer to initial addresses of the word storage slots.

The process operates read/write circuitry to read a first word from a word storage slot indicated by the initial read pointer address into scan storage circuitry that is separate from the word storage slots.

The process shifts the scan storage circuitry to shift the first word out of the scan storage circuitry and simultaneously shift a second word into the scan storage circuitry.

The process operates the read/write circuitry to write the second word from the scan storage circuitry into a word storage slot indicated by the initial write pointer address.

None of the Jagger, Campbell, or Freidin patents disclose operating a data read/write circuit to read data between word storage slots of a FIFO memory and a serially shifted scan storage circuitry.

New claim 29 distinguishes over the Jagger, Campbell, and Freidin patents with the limitations of a process of scan testing a first-in first-out memory having word storage slots, comprising: setting a read pointer and a write pointer to initial addresses of the word storage slots; operating read/write circuitry to read a first word from a word storage slot indicated by the initial read pointer address into scan storage circuitry that is separate from the word storage slots; shifting the scan storage circuitry to shift the first word out of the scan storage circuitry and simultaneously shift a second word into the scan storage circuitry; and operating the read/write circuitry to write the second word from the scan storage circuitry into a word storage slot indicated by the initial write pointer address.

The depending claims also stand allowable as depending from allowable independent claims 25 and 29 and as including, in combination

with the limitations of the independent claims, additional distinguishing limitations.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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